REMARKS

Claims 1 - 8 have been cancelled. Claims 9 - 16 have been added. Reconsideration of this application in view of the amendments noted is respectfully requested.

Claims 9 - 16 generally correspond to now cancelled claims 1 - 8. In other words, claim 9 corresponds to cancelled claim 1, claim 10 corresponds to cancelled claim 2, etc. The claims have in effect been amended to correct errors caused by translation to the English language, to employ consistent terminology, to correct any lack of antecedent basis, and to correct any other informalities.

In the Office Action, claims 1 - 8 were rejected under 35 U.S.C. Section 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Office Action states that claim 1 recites "cables for interconnecting the local time counters to the pulse generator module" and that the system is characterized by "multiple time counters that comprises one or more pulse generator modules." The examiner therefore understands this to mean that a component of the local time counter (pulse generator) is connected to the local time counter by a cable, but the specification appears to teach that the cable is used to connect a singe pulse generator module to a number of other processors in a cluster.

Claim 9 is in effect an amendment of claim 1. In claim 9, it is clear that the distributed global clock includes a plurality of pulse generator modules and a plurality of local time counter modules. The plurality of pulse generator modules are interconnected to form a hierarchical structure, and one of the pulse generator modules (a single pulse generator module) is at the top of the hierarchical structure. Therefore, it is clear that the "single pulse generator module" is therefore connected to all of the other pulse generator modules of the cluster that are below it in the hierarchical structure, as described in the specification in the paragraph beginning on page 3, line 27. Further, a plurality of interconnecting cables interconnect the local time counter modules to the pulse generator modules. These features are also shown in FIGS. 1 and 2 of the drawings.

For these reasons, applicant submits that the limitations of claim 9 comply with the written description requirement. Therefore, applicant respectfully requests that the Section 112, first paragraph rejection be withdrawn.

Claims 1 - 8 were rejected under 35 U.S.C. Section 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More particularly, certain limitations in the claims were found to lack sufficient antecedent basis, and other terminology in the claims appeared to be inconsistently worded and therefore created confusion as to what limitations were being referred to.

As stated above, new claims 9 - 16 are effectively amended versions of now cancelled claims 1 - 8. New claims 9 - 16 have been written with a view towards eliminating any lack of antecedent basis found in the claims and to assure that the terminology used in the claims is consistent. Hence, applicant submits that claims 9 - 16 use consistent terminology, and that there is sufficient antecedent basis for all of the limitations of claims 9 - 16. Therefore, applicant respectfully requests that the Section 112, second paragraph rejection be withdrawn.

Claim 1 was rejected under 35 U.S.C. Section 102(b) as being anticipated by Parry et al. (U.S. Patent No. 5,822,381, hereinafter "Parry"). Applicant respectfully traverses this rejection.

Parry fails to disclose local time counter modules that only receive clock signals and do not generate clock signals, as in the present invention. In independent claim 9, a single pulse generator module at the top of a hierarchical structure of interconnected pulse generator modules generates clock pulses that are sent down through the hierarchical structure, and a plurality of local time counter modules are incremented by the pulses sent by the single pulse generator module. Instead, in Parry, a plurality of local clock means generate a global clock source signal (see, for example, column 9, lines 36 - 37).

Further, Parry fails to disclose that a single pulse generator module generates clock pulses that are sent down through the hierarchical structure of pulse generator modules, as

in claim 9. Instead, in Parry, a router means, in the distribution network, receives global clock source signals from a plurality of local clock means, selects one of the global clock source signals as a global clock signal, and provides the global clock signal to the distribution network (see, for example, column 9, lines 46 - 50).

Furthermore, Parry fails to disclose that the length of the interconnecting cables interconnecting the local time counter modules to the pulse generator modules guarantees that the counters of all the local time counter modules are incremented synchronously, as in claim 9. Instead, in Parry each local clock means must have a filter (mask means) capable of generating a sampling window precisely adjusted for capturing the transition of the global clock signal and increment a counter. More specifically, the mask means generates a periodic sampling window having a frequency equal to a frequency of the global clock signal and having a length corresponding to a portion of a period of the global clock signal, and increment means that produce a counter increment signal in response to receipt of an edge of the global clock signal during the sampling window (see, for example, column 10, lines 1 - 8).

Moreover, Parry fails to disclose that the counters of the local time counter modules are incremented directly by the pulses coming from the pulse generator modules, as in claim 9.

Even more, Parry fails to disclose that any local time counter module can send a reset signal provided by its associated processing node to the hierarchical structure of pulse generator modules for simultaneous initialization of all the local time counter modules, as in claim 9. In the present invention, the local time counter module providing the reset signal sends the reset signal up through the hierarchical structure of pulse generator modules, the reset signal reaches the single pulse generator at the top of the hierarchical structure, and is sent back down through the hierarchical structure reaching all of the local time counter modules simultaneously. On arrival from the pulse generator modules, the reset signal initializes the counters of all of the local time counter modules simultaneously and, after such initialization, the pulses generated by the single pulse generator at the top of

the hierarchical structure synchronously increment the counters of all the local time counter modules of the distributed global clock. These features of claim 9 are not disclosed by Parry. Instead, in Parry, global clock initialization requires a means for disabling the global clock source signal, a means for setting the counters to a specific value, a means for disabling the filter capable of generating a sampling window precisely adjusted for capturing the transition of the global clock signal that increments the counters, and a means for enabling the filter after the reception of the first edge of the global clock signal (see, for example, column 10. line 53 through column 11, line 3).

For these reasons, applicant submits that the limitations of claim 9 and its dependencies are not disclosed by Parry. Therefore, applicant respectfully requests that the Section 102(b) rejection based upon Parry be withdrawn.

This amendment and request for reconsideration is felt to be fully responsive to the comments and suggestions of the examiner and to place this application in condition for allowance. Favorable action is requested.

Respectfully submitted,

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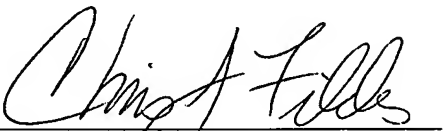

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